REMARKS

The Office Action of July 31, 2002 was received and carefully reviewed. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Filed concurrently herewith is a *Request for a One Month Extension of Time* which extends the shortened statutory period of response to November 30, 2002. Accordingly, Applicants respectfully submit that this response is being timely filed.

Claims 1-38 were pending prior to the instant amendment. By this amendment, claims 1-9, 11, 13-15, 17-23, 25-27, 29, 31-33 and 35-36 are amended, and claims 10 and 28 are canceled herein. Consequently, claims 1-9, 11-27 and 29-38 are now pending in the instant application.

Initially, the drawings are objected to for failing to properly designate that which is old with a legend, such as "Prior Art." In response thereof, Figures 2A, 2B, 5, 6A and 6B are amended in a *Request for Drawing Changes* filed simultaneously herewith to include the noted legend in order to overcome this objection.

The specification is also objected to on page 5 for referring to a "register line selecting switch 103" where item 103 is a register group. Applicants amend the third paragraph on page 5 in order to overcome this objection.

Claims 1-38 are rejected under 35 U.S.C. 112, first paragraph, for allegedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one of skill in the art that the inventor had possession of the invention at the time of filing the claimed invention. This rejection is traversed for the reasons advanced in detail below.

Specifically, the Examiner contends that the phrase "a crystalline semiconductor layer" cannot be found in the specification. As can be seen from the attached definition of "crystalline" from the *McGraw-Hill Dictionary of Scientific and Technical Terms*, this term merely means "of, or pertaining to, resembling or composed of crystals." As a result, there is nothing to suggest in this definition that the term must be "single" crystalline as asserted by the Examiner. Instead, the "crystalline" semiconductor layer may include polycrystalline. Furthermore, Applicants note that numerous prior patents have been issued with this very same language even when the specification did not

expressly disclose a single crystalline semiconductor. Consequently, Applicants believe the Examiner is being too restrictive with regard to this term, and, thus, should reconsider and withdraw this rejection.

With regard to claims 13, 17, 31 and 35, the phrase "CMOS circuit" is considered improper under Section 112, first paragraph, since this phrase cannot be found in the original text. Although the specification does not appear to expressly utilize this phrase, Applicants contend that the specification inherently teaches a CMOS circuit, for example, at Figures 10A-10F, wherein a method of forming a complementary invertor is clearly illustrated to support the recitation of a CMOS circuit.

With regard to claims 10 and 28, these claims are canceled, thus, rendering this aspect of the rejection moot.

Claims 1-38 are rejected under 35 U.S.C. 112, second paragraph, for being indefinite. Claims 1-9, 11, 13-15, 17-23, 25-27, 29, 31-33 and 35-36 are amended herein to overcome this rejection.

Specifically, the above-noted claims are amended to remove the "type" language found objectionable by the Examiner. For example, support for the term "p-channel transistors" is provided at least on page 17, line 23 of the specification. In other case, the term "type" is merely removed from the claims. As a result, this aspect of the rejection should be considered overcome.

Further, the Examiner contends that the term "CMOS" would not be understood by one of skill in the art. Applicants do not agree with this contention, since the term has clear meaning to one of skill in the art in the context of a semiconductor device. A definition of "CMOS" as a complementary metal-oxide semiconductor is provided herewith from *The IEEE Standard Dictionary of Electrical and Electronics Terms* to support this contention. Thus, this rejection is believed to be overcome, and reconsideration and withdrawal of this rejection are respectfully requested.

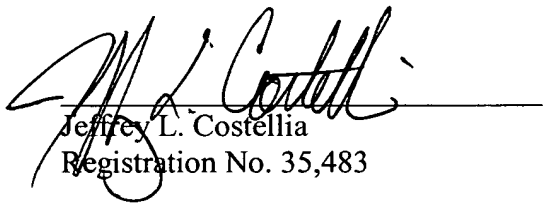
Claims 1-38 are rejected under 35 U.S.C. 102(e) over the reference to Matsumoto (5,323,042). This rejection is traversed for the reasons advanced in detail below.

The Examiner alleges that Matsumoto teaches a display medium capable of electrically changing luminous strength. Applicant was unable to find such a teaching. As a result, the Examiner is requested to expressly provide reference to such a teaching in

Matsumoto is this rejection is maintained. Applicants understand that a display medium capable of electrically changing luminous strength is, for example, a light emitting material, such as an electroluminescence material. Since Matsumoto is directed to a liquid crystal device, this rejection is not believed to be appropriate because the reference fails to teach each and every feature of the claimed invention. Claims 1, 7, 13, 17, 19, 25, 31, and 35 recite this display medium feature, and thus, these claims, as well as the claims depending therefrom, should be considered allowable over the cited Matsumoto patent.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-9, 11-27 and 29-38 be allowed and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



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MARKED UP VERSION

--As shown in Fig. 1, a shift register circuit 104 includes at least one register group 103 and a register selecting switch 102. The register group includes register lines 101a, 101b, . . . , and 101n having a plurality of serial-connected registers SRAi, SRBi, . . . , and SRZi (i = 1 to n), respectively. The register line selecting switch 102 [103] selects one of the register lines.--

1. (Amended) An active matrix [type] display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements,

wherein each of said plurality of thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film.

2. (Amended) The active matrix [type] display device according to claim 1 wherein said gate electrode is located over said semiconductor layer.

3. (Amended) The active matrix [type] display device according to claim 1 wherein all of said plurality of thin film transistors are p-channel transistors [p-type].

4. (Amended) The active matrix [type] display device according to claim 1 wherein all of said plurality of thin film transistors are n-channel transistors [n-type].

5. (Amended) The active matrix [type] display device according to claim 1 wherein said substrate is a glass substrate.

7. (Amended) An active matrix [type] display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements, wherein each of said plurality of thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film,

wherein said crystalline semiconductor layer has source and drain regions and at least one lightly doped region.

8. (Amended) The active matrix [type] display device according to claim 7 wherein said substrate is a glass substrate.

9. (Amended) The active matrix [type] display device according to claim 7 wherein said source and drain regions and said at least one lightly doped region are doped with phosphorus.

11. (Amended) The active matrix [type] display device according to claim 7 wherein said gate electrode is located over said semiconductor layer.

13. (Amended) An active matrix [type] display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a CMOS circuit comprising at least one n-channel [type] thin film transistor and one p-channel [type] thin film transistor,

wherein each of said n-channel and p-channel [type] thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film.

14. (Amended) The active matrix [type] display device according to claim 13 wherein said substrate is a glass substrate.

15. (Amended) The active matrix [type] display device according to claim 13 wherein said gate electrode is located over said semiconductor layer.

17. (Amended) An active matrix [type] display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a CMOS circuit comprising at least one n-channel [type] thin film transistor and one p-channel [type] thin film transistor, each of said first and second thin film transistors comprising a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film,

wherein said crystalline semiconductor layer has source and drain regions and at least one lightly doped region.

18. (Amended) The active matrix [type] display device according to claim 19 wherein said substrate is a glass substrate.

19. (Amended) An active matrix [type] display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements,

wherein each of the film transistors of said switching elements and said driver circuit comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film.

20. (Amended) The active matrix [type] display device according to claim 19 wherein said gate electrode is located over said semiconductor layer.

21. (Amended) The active matrix [type] display device according to claim 19 wherein all of said plurality of thin film transistors are p-channel transistors [p-type].

22. (Amended) The active matrix [type] display device according to claim 19 wherein all of said plurality of thin film transistors are n-channel transistors [n-type].

23. (Amended) The active matrix [type] display device according to claim 19 wherein said substrate is a glass substrate.

25. (Amended) An active matrix [type] display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements,

wherein each of the thin film transistors of the switching elements and the driver circuit comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film,

wherein said crystalline semiconductor layer has source and drain regions and at least one lightly doped region.

26. (Amended) The active matrix [type] display device according to claim 25 wherein said substrate is a glass substrate.

27. (Amended) The active matrix [type] display device according to claim 25 wherein said source and drain regions and said at least one lightly doped region are doped with phosphorus.

29. (Amended) The active matrix [type] display device according to claim 25 wherein said gate electrode is located over said semiconductor layer.

31. (Amended) An active matrix [type] display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a CMOS circuit comprising at least one n-channel [type] thin film transistor and one p-channel [type] thin film transistor,

wherein each of the film transistors of the switching elements and said n-channel and p-channel [type] thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film.

32. (Amended) The active matrix [type] display device according to claim 31 wherein said substrate is a glass substrate.

33. (Amended) The active matrix [type] display device according to claim 31 wherein said gate electrode is located over said semiconductor layer.

35. (Amended) An Active matrix [type] display device comprising:

a substrate having an insulating surface;

a plurality of pixel electrodes arranged in a matrix form over said substrate;

a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor;

a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes; and

a CMOS circuit comprising at least one n-channel [type] thin film transistor and one p-channel [type] thin film transistor,

wherein each of the film transistors of the switching elements and said n-channel and p-channel [type] thin film transistors comprises a crystalline semiconductor layer, a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film, and said crystalline semiconductor layer has source and drain regions and at least one lightly doped region.

36. (Amended) The active matrix [type] display device according to claim 35 wherein said substrate is a glass substrate.